IN THE CLAIMS:

1. **(Currently amended)** Process for generating a feed-through in a semiconductor wafer~~,~~ which has electric circuitry embedded in a front surface ~~wereby the~~ whereby a hole for the feed-through is generated by the combined use of a front side protection layer and a wet KOH etch process etching the hole from ~~the~~a back side of the wafer, where a photomaking process is subsequently used do define ~~the~~ vias followed by deposition of ~~the~~ via material.

2. **(Original)** Process as claimed in claim 1, where the front side protection layer comprises: a) an electrical insulation layer, preferably a PECVD silicon nitride layer; b) a KOH resistant metallic layer, preferably a TiW layer and an Au layer.

3. **(Currently amended)** Process as claimed in ~~claims 1-2~~ claim 1, whereby the etch process from the back side takes place in a number of steps:

- a KOH etch resistant layer is deposited on the back side,
- openings for the through-holes are defined in the KOH etch resistant layer using a photomasking process in alignment with the circuitry embedded in the front side silicon,
- the openings for the through-holes are etched in the KOH resistant layer, and
- the through-holes are in the silicon are etched in a KOH bath.

4. **(Original)** Process as claimed in claim 3, whereby the front side electric insulation and the KOH etch-resistant metallic layers covering

the through-holes are etched from the back side through the formed holes in the silicon.

5. **(Original)** Process as claimed in claim 3, whereby the front side electric insulation and the KOH etch-resistant metallic layers covering the through-holes are etched from the front side, preferably using a photomasking process in alignment with the through-holes.

6. **(Currently amended)** Process as claimed in ~~claim 4 or~~ claim 5, whereby the inside of the etched holes and back side of the wafer are covered with an insulation layer, preferably a PECVD deposited insulation layer, and the insulation layer is covered with a plating base, preferably by deposition of a TiW adhesion layer and an Au layer.

7. **(Original)** Process as defined in claim 6, where residual insulation material on the front side originating from the PECVD process on the back side, especially in the areas around the holes is removed, preferably by sputter etching.

8. **(Original)** Process as defined in claim 1, whereby the photomasking process comprises deposition of an electrodeposited photoresist, whereby the deposited photoresist is exposed through a mask defining the negative image of the feed-through back and front side respectively and where the photoresist is developed and the feed-through is subsequently formed by deposition of metal.

9. **(Original)** Process as claimed in claim 8, whereby the feed-through is formed by deposition of Cu and Ni.

10. **(Currently amended)** Amplifier produced according to ~~one or more of the claims 1-9~~ claim 1, wherein terminals for gaining contact with

the CMOS structure embedded in the surface of a front side of semiconductor wafer are placed on both back and front sides of the wafer and where a feed-through connects the terminals on the back side with the CMOS circuitry embedded in the front side of the wafer.